Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A VDD-to-VSS clamp circuit comprising:
a power node driven by a power supply;
a ground node for coupling to a ground supply;
a shunt transistor that conducts current from the power node to the ground node in response to a gate node;
a buffer that drives the gate node in response to a trigger node;
a resistor and a capacitor in series between the power node and the ground node, with the trigger node between the resistor and the capacitor; and
a feedback transistor, having a gate driven by the gate node, for conducting current to the trigger node,
whereby the shunt transistor conducts current between the power node and the ground node to protect other circuits connected between the power node and the ground node.

[c2] 2.The VDD-to-VSS clamp circuit of claim 1 wherein the feedback transistor conducts current in parallel to the resistor,
whereby the feedback transistor prevents a large voltage difference between the power node and the trigger node

when the feedback transistor is turned on.

[c3] 3.The VDD-to-VSS clamp circuit of claim 2 wherein the feedback transistor hardens the VDD-to-VSS clamp circuit from latch-up by ensuring that the shunt transistor is in an off state under a normal powered condition when the feedback transistor is turned on.

[c4] 4.The VDD-to-VSS clamp circuit of claim 3 wherein the resistor is formed in an N-well.

[c5] 5.The VDD-to-VSS clamp circuit of claim 3 wherein the feedback transistor conducts current to the trigger node when the shunt transistor is turned off.

[c6] 6.The VDD-to-VSS clamp circuit of claim 2 wherein the feedback transistor and the resistor are each coupled between the power node and the trigger node.

[c7] 7.The VDD-to-VSS clamp circuit of claim 6 wherein the feedback transistor is a p-channel feedback transistor.

[c8] 8.The VDD-to-VSS clamp circuit of claim 7 wherein the shunt transistor is an n-channel transistor.

[c9] 9.The VDD-to-VSS clamp circuit of claim 8 wherein the buffer is an inverter that inverts the trigger node to generate the gate node.

[c10] 10.The VDD-to-VSS clamp circuit of claim 9 wherein the buffer comprises a p-channel pull-up transistor and an n-channel pull-down transistor having drains driving the gate node and gates driven by the trigger node.

[c11] 11.The VDD-to-VSS clamp circuit of claim 2 wherein the capacitor is connected between the trigger node and the ground node.

[c12] 12.A protective circuit comprising:
shunt means, connected between a first and a second supply line, for shunting current between the first and second supply line in response to a gate signal;
buffer means for generating the gate signal in response to a trigger signal;
time-constant means, coupled between the first and second supply lines, for initially holding the trigger signal at a first state when a discharge occurs to the first supply line, and for driving the trigger signal to a second state after a timed delay when the discharge occurs; and
feedback means, coupled to drive the trigger signal and responsive to the gate signal, for driving the trigger signal to the second state when no discharge occurs,
whereby the feedback means drives the trigger signal to prevent accidental triggering of the protective circuit.

[c13] 13.The protective circuit of claim 12 wherein the feed-

back means is connected to conduct current between the first supply line and the trigger signal.

[c14] 14.The protective circuit of claim 12 wherein the shunt means comprises a shunt transistor between the first and second supply lines;
wherein the buffer means comprises inverter means for inverting a state of the trigger signal to generate the gate signal;
wherein the feedback means comprises a feedback transistor of an opposite type as a type of the shunt transistor.

[c15] 15.The protective circuit of claim 14 wherein the time-constant means comprises:
a resistor coupled between the first supply line and the trigger signal; and
a capacitor coupled between the second supply line and the trigger signal,
wherein the feedback means drives the trigger signal to the second state before the timed delay of the resistor and capacitor.

[c16] 16.The protective circuit of claim 15 wherein the shunt transistor is an n-channel transistor and wherein the feedback transistor is a p-channel transistor.

[c17] 17.The protective circuit of claim 16 wherein the first supply line is coupled to a power supply and the second supply line is coupled to a ground.

[c18] 18.The protective circuit of claim 17 wherein the resistor is formed in an N-well that can collect electrons injected by an n+ region that pass through a p-substrate region, wherein the feedback means reduces a voltage drop within the N-well when the N-well collects electrons, whereby latch-up susceptibility of the resistor is reduced by the feedback means.

[c19] 19.An electro-static-discharges (ESD) clamp circuit comprising:

a power node;

a ground node;

a shunt transistor having a channel between the power node and the ground node and a gate connected to a gate node;

a stage having a trigger node as an input and the gate node as an output;

a resistor connected between the power node and the trigger node;

a capacitor connected between the ground node and the trigger node;

a feedback transistor having a gate connected to the gate node and a drain connected to the trigger node.

[c20] 20.The electro-static-discharges (ESD) clamp circuit of claim 19 wherein the feedback transistor is a p-channel with a source connected to the power node;
wherein the shunt transistor is an n-channel transistor with a drain connected to the power node and a source connected to the ground node;
wherein the stage comprises a p-channel transistor and an n-channel transistor in series between the power node and the ground node with drains driving the gate node and gates connected to the trigger node.